

**IN THE CLAIMS:**

Please cancel claims 10-18 without prejudice to or disclaimer of the subject matter recited therein.

Please amend claims 1-4, 6, and 8-9 as follows:

**LISTING OF CURRENT CLAIMS**

Claim 1. (Currently Amended) A package substrate for improving electrical performance comprising:

a first insulating layer having a top surface and a bottom surface;

5 a plurality of groups of inner fingers formed on the top surface of the first insulating layer for electrically connecting to a chip;

a plurality of outer fingers formed on the top surface of the first insulating layer for electrically connecting to the chip;

a plurality of outer through holes formed through the first insulating layer and electrically connected to the corresponding outer fingers;

10 a plurality of inner through holes formed through the first insulating layer and electrically connected to the corresponding inner fingers; and

a ground/power layer ~~disposed~~ located on the bottom surface of the first insulating layer, ~~wherein the ground/power layer has~~ and having a plurality of openings, ~~and the inner through holes are crowded in groups to pass through the openings which are electrically isolated from the ground/power layer.~~ wherein a group of the inner through holes including at least two of the inner through holes passes through and is corresponding to one of the plurality of openings to be electrically isolated from the ground/power layer.

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Claim 2. (Currently Amended) The substrate in accordance with claim 1, wherein a distance between ~~the~~ two adjacent openings of the plurality of openings is not less than 0.2mm.

Claim 3. (Currently Amended) The substrate in accordance with claim 1, wherein the ground/power layer between two adjacent openings of the plurality of openings is in strip shape.

Claim 4. (Currently Amended) The substrate in accordance with claim 1, wherein ~~each group of a plurality of groups of the~~ inner through holes pass through the corresponding openings and are arranged in grid array: a radial arrangement.

Claim 5. (Original) The substrate in accordance with claim 1, wherein the top surface of the first insulating layer includes a chip-attaching region.

Claim 6. (Currently Amended) The substrate in accordance with claim 5, wherein the plurality of openings are radially oriented to the chip-attaching region.

Claim 7. (Original) The substrate in accordance with claim 5, further comprising a metal ring formed on the top surface of the first insulating layer between the chip-attaching region and the inner fingers.

Claim 8. (Currently Amended) The substrate in accordance with claim 1, further comprising a second insulating layer formed ~~on~~ below the bottom surface of the first insulating layer ~~to sandwich the ground/power layer: layer located between the first insulating layer and the second insulating layer.~~

Claim 9. (Currently Amended) The substrate in accordance with claim 8, further comprising another ground/power layer on ~~the~~ a bottom surface of the second insulating layer.

Claims 10-18. (Canceled)